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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/594,091	06/15/2000	Akio Itoh	000761	8583

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EXAMINER
WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
2815	18

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/594,091	ITOH	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on November 27, 2002.

Claim Objections

Claims 1, 5, 12, and 13 are objected to because of the following informalities: Each independent claim includes the limitation "the silicon nitride film including nitrogen." The is insufficient antecedent basis for the limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita et al. (US 6,046,490) in view of Zhang (US 5,990,491).

Arita shows (fig. 1) a semiconductor device comprising a transistor having a first and second impurity region (3) formed in a substrate (1), and a gate electrode (5). A first insulating layer (6) covers the transistor. A capacitor (10) is formed on the insulating layer, the capacitor having a dielectric (8) formed of a high dielectric constant material (col. 8, lines 39-45), and an upper electrode (9) and lower electrode (7) with the

dielectric positioned therebetween. A silicon oxide film (22) is formed over the capacitor and has its upper surface planarized. A silicon nitride oxide film (14), which contains some nitrogen, is formed on the oxide to prevent moisture from penetrating the device (col. 6, lines 10-17). A second insulating film (15) is formed between the capacitor and the silicon oxide film. Arita et al. does not specifically show that a contact is positioned above the silicon nitride film including nitrogen. Although it is well known in the art to form a contact above a passivation layer to provide electrical connection to the semiconductor device, Zhang shows (fig. 5) a semiconductor device having a lower oxide insulating layer (509), a passivation layer of silicon nitride (514), and a contact (510) formed over the passivation layer. The contact provides an electrical connection to the lower semiconductor components through the insulation layers (col. 7, lines 44-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Arita by adding an upper contact above the silicon nitride passivation film as taught by Zhang to provide an electrical connection to the lower semiconductor components.

Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arita et al. (US 6,046,490) and Zhang (US 5,990,491) as applied to claim 1 above, and further in view of Singh et al. (US 5,847,464).

Arita and Zhang show of the element of the claims except the cavities formed in the silicon oxide film. Singh et al. discloses a semiconductor device comprising an interlevel dielectric layer (46) which has cavities (voids 72, 74, etc) formed throughout the layer (see fig. 3b). The cavities help lower the capacitance and ultimately helps

reduce RC delay of signals along adjacent metal lines (col. 5 lines 57-67, col. 6, lines 48-64). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor capacitor of Arita and Zhang by forming cavities in the silicon oxide layer as taught by Singh to reduce capacitance and lower delay of signals along metal signal lines.

Claims 5, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. (US 5,990,507) in view of Arita et al. (US 6,046,490) and Zhang (US 5,990,491).

Mochizuki et al. shows (fig. 17) a semiconductor device comprising a transistor having a first and second impurity region (S, D) formed in a substrate (1), and a gate electrode (G, 4 & 5). A first insulating layer (10) covers the transistor. A capacitor is formed on the insulating layer, the capacitor having a dielectric (18) formed of a ferroelectric material, and an upper electrode (19) and lower electrode (17) with the dielectric positioned therebetween. A second insulating film (13) is formed on the capacitor. A local interconnection (22) is formed on the second insulating film for connecting the upper electrode of the capacitor to the first impurity region (S). Third insulating film (30) is formed on the local interconnection and the second insulating film. A first wiring (BL) is formed on the third insulating film and electrically connects to the second impurity region (D)via a hole which is formed in the first, second, and third insulating films. A fourth insulating film (39) is formed on the first wiring and has a planarized upper surface. The upper surface of the first insulating film is planarized. A

second wiring is formed on the fourth film and connects to the first wiring via a hole formed through the fourth insulating layer (col. 24, lines 49-67). Mochizuki shows all of the elements of the claims except the third and fourth insulating films formed specifically of silicon oxide. Arita shows (fig. 1) a semiconductor device comprising a transistor having a capacitor device covered by third and fourth insulating films, which are formed of silicon oxide (col. 6, lines 1-17). A silicon nitride oxide film (14) is formed on the oxide. With this configuration, moisture is prevented from penetrating the device (col. 6, lines 10-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulating layers Mochizuki by forming oxide and then oxynitride as taught by Arita to prevent moisture from penetrating the device.

Mochizuki et al. and Arita et al. do not specifically show that a contact is positioned above the silicon nitride film including nitrogen. Although it is well known in the art to form a contact above a passivation layer to provide electrical connection to the semiconductor device, Zhang shows (fig. 5) a semiconductor device having a lower oxide insulating layer (509), a passivation layer of silicon nitride (514), and a contact (510) formed over the passivation layer. The contact provides an electrical connection to the lower semiconductor components through the insulation layers (col. 7, lines 44-50). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Mochizuki and Arita by adding an upper contact above the silicon nitride passivation film as taught by Zhang to provide an electrical connection to the lower semiconductor components.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. (US 5,990,507) in view of Arita et al. (US 6,046,490) and Zhang (US 5,990,491), as applied to claim 5 above, and further in view of Singh et al. (US 5,847,464).

Mochizuki, Arita, and Zhang show all of the elements of the claims except the cavities exposed from an upper surface of the insulating film. Singh et al. shows (fig. 5 a-c) cavities (76, 78, 76", 78") in an upper insulating film (46) which are partially exposed from the film. Another insulating film (80) is formed on the first insulating (46) film to cover the cavities. The cavities help lower the capacitance and ultimately helps reduce RC delay of signals along adjacent metal lines (col. 5 lines 57-67, col. 6, lines 48-64). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor capacitor of Mochizuki, Arita, and Zhang by forming cavities in the silicon oxide layer as taught by Singh to reduce capacitance and lower delay of signals along metal signal lines.

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703)

305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW
MEW
February 6, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800